Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	(("6,397,114") or ("6,326,758") or ("5, 442,555")).PN.	US-PGPUB; USPAT	OR	OFF	2004/12/26 19:57

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((((pump AND "artificial neural") AND fault) AND detect) AND power): 37 patents.
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	PAT. NO.	Title
1	6,826,426	Objective pain signal acquisition system and processed signal
2	6,823,244	Vehicle part control system including electronic sensors
3	6,785,636	Fault diagnosis in a complex system, such as a nuclear plant, using probabilistic reasoning
4	6,768,920	System for delivering pain-reduction medication
5	6,757,665	Detection of pump cavitation/blockage and seal failure via current signature analysis
6	6,751,499	Physiological monitor including an objective pain measurement
7	6,738,697	Telematics system for vehicle diagnostics
8	6,735,506	Telematics system
9	6,733,036	Automotive electronic safety network
10	6,654,697	Flow measurement with diagnostics
11	6,654,632	System for processing a subject's electrical activity measurements
12	6,648,367	Integrated occupant protection system
13	6,646,397	Integrated control and diagnostics system
14	6,633,782	Diagnostic expert in a process control system
15	6,625,569	Real-time spatio-temporal coherence estimation for autonomous mode identification and invariance tracking
16	6,539,267	Device in a process system for determining statistical parameter
17	6,533,316	Automotive electronic safety network
18	6,532,392	Transmitter with software for determining when to initiate diagnostics
19	6,529,135	Integrated electric motor monitor
20	6,484,080	Method and apparatus for controlling a vehicular component
21	6,418,424	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system
22	6,415,276	Bayesian belief networks for industrial processes

23 6,397,114 Device in a process system for detecting events
24 6,326,758 Integrated diagnostics and control systems
25 6,216,118 Apparatus and method for discriminating a time series data
26 6,202,473 Gas sensor with protective gate, method of forming the sensor, and method of sensing
27 6,182,500 Gas sensor with protective gate, method of forming the sensor, and method of sensing
28 6,175,787 On board vehicle diagnostic module using pattern recognition
29 6,155,100 Gas sensor with protective gate, method of forming the sensor, and method of sensing
30 6,119,111 Neuro-parity pattern recognition system and method
31 6,119,047 Transmitter with software for determining when to initiate diagnostics
32 6,017,143 Device in a process system for detecting events
33 5,995,910 Method and system for synthesizing vibration data
34 5,920,477 Human factored interface incorporating adaptive pattern recognition based controller apparatus
35 5,875,108 Ergonomic man-machine interface incorporating adaptive pattern recognition based control system
36 5,774,357 Human factored interface incorporating adaptive pattern recognition based controller apparatus
37 5,442,555 Combined expert system/neural networks method for process fault diagnosis

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Terms used **pump** and **artificial neural** and **fault** and **detect** and **power**

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1 Real time application of artificial neural network for incipient fault detection of induction machines

Mo-yuen Chow, Sui Oi Yee

June 1990 **Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2**

Full text available: pdf(751.83 KB) Additional Information: full citation, abstract, references, index terms

This paper describes several artificial neural network architectures for real time application in incipient fault detection of induction machines. The artificial neural networks perform the fault detection in real time, based on direct measurements from the motor, and no rigorous mathematical model of the motor is needed. Different approaches used to develop a reliable fault detector are presented and compared in this paper. The designed networks vary in complexity and accuracy. A high-orde ...

2 An object-oriented expert system for coal-fired MHD power plant fault monitoring and diagnosis

Eddie S. Washington, Moonis Ali

June 1989 **Proceedings of the second international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(585.54 KB) Additional Information: full citation, abstract, references, index terms

Abnormal process behaviors observed through sensor data values are symptomatic of process faults. It has been demonstrated that pattern recognition techniques that associate faults with the symptoms they produce can be successfully applied in performing on-line automated fault detection and diagnosis [1-3]. This paper describes an object-oriented implementation of a knowledge-based expert system designed to aid power plant operators by performing automated sensor based fault detection and d ...

3 Software safety: why, what, and how

Nancy G. Leveson

June 1986 **ACM C mputing Surveys (CSUR)**, Volume 18 Issue 2

Full text available: pdf(4.18 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Software safety issues become important when computers are used to control real-time,

safety-critical processes. This survey attempts to explain why there is a problem, what the problem is, and what is known about how to solve it. Since this is a relatively new software research area, emphasis is placed on delineating the outstanding issues and research topics.

4 Diagnosis of power plant faults using qualitative models and heuristic rules

Irina Obreja

June 1990 **Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(553.41 KB) Additional Information: full citation, abstract, references, index terms

This paper presents results obtained in an AI research effort in the industrial field of Nuclear Power Plants (NPP): malfunction diagnosis of the Emergency Feedwater System (EFWS) of a NPP. An expert system was developed which utilizes qualitative techniques for modeling the system and heuristic rules for generating causal explanations of an observed malfunction. The operation of the system, the model and the global inference mechanism are discussed. Another purpose of the paper is to prese ...

5 LEADER-an integrated engine behavior and design analyses based real-time fault diagnostic expert system for space shuttle main engine (SSME)

U. K. Gupta, M. Ali

June 1989 **Proceedings of the second international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, index terms

An expert system, called LEADER, has been designed and implemented for automatic learning, detection, identification, verification and correction of anomalous propulsion system operations in real time. LEADER employs a set of sensors to monitor engine component performance, and to detect, identify and validate abnormalities with respect to varying engine dynamics and behavior. Two diagnostic approaches are adopted in the architecture of LEADER. In the first approach fault diagnosis is perfo ...

6 Applications of qualitative modeling to knowledge-based risk assessment studies

Gautam Biswas, Kenneth A. Debelak, Kazuhiko Kawamura

June 1989 **Proceedings of the second international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(729.63 KB) Additional Information: full citation, abstract, references, citings, index terms

Risk assessment of technological processes (chemical and power plants, electro-mechanical systems) is a complex process that requires enumeration of all possible failure modes, their probability of occurrence, and their consequences. Traditionally such studies have been performed by a committee of expert engineers with diverse backgrounds. This paper discusses the use of qualitative modeling techniques based on deriving behavior from structural descriptions and causal reasoning to aid autom ...

7 Diagnosing multiple faults using knowledge about malfunctioning behavior

Tim Hansen

June 1988 **Pr ceedings f the first internati nal c nference n Industrial and engineering applicati ns of artificial intelligence and expert systems - V lume 1**

Full text available: pdf(647.72 KB) Additional Information: full citation, abstract, references, index terms

A technical fault diagnosis system based on knowledge about the structure of a device and

the behavior of its components is presented. This approach allows knowledge about components to be reused for new devices and simplifies maintenance of the fault diagnosis system. A new method for diagnosing multiple faults using this representation is presented and discussed. The method assumes that both normal functioning and malfunctioning behavior are described for components in the form of user-de ...

8 DPRL: a language for representation of operation and safety maintenance procedures of nuclear power plants

Rajiv Bhatnagar, D. W. Miller, B. K. Hajek, B. Chandrasekaran

June 1990 **Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2**

Full text available: pdf(870.34 KB) Additional Information: full citation, references, citings, index terms

9 Efficient analog test methodology based on adaptive algorithms

Luigi Carro, Marcelo Negreiros

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(225.70 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This papers describes a new, fast and economical methodology totest linear analog circuits based on adaptive algorithms. To theauthors knowledge, this is the first time such technique is used totest analog circuits, allowing complete fault coverage. The paperpresents experimental results showing easy detection of soft,large-deviation and hard faults, with low cost instrumentation.Components variations from 5% to 1% have been detected, asthe comparison parameter (output error power) varied from30 ...

10 On accuracy of switch-level modeling of bridging faults in complex gates

R. Rajsuman, Y. K. Malaiya, A. P. Jayasumana

October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**

Full text available: pdf(814.83 KB) Additional Information: full citation, abstract, references, citings, index terms

Bridging faults have been shown to be a major failure mode in VLSI devices. This study examines nMOS and CMOS complex gates in detail for bridging faults. Analysis is carried out using both switch and circuit level models for comparison. It is shown that in most cases, the switch level analysis predicts the correct behavior. A set of conditions are presented, under which the switch level analysis may fail to predict the correct behavior. These conditions can be used for accurate switch leve ...

11 Illustrative risks to the public in the use of computer systems and related technology

Peter G. Neumann

January 1996 **ACM SIGSOFT Software Engineering Notes**, Volume 21 Issue 1

Full text available: pdf(2.54 MB) Additional Information: full citation

12 Human-Computer Interaction in the Control of Dynamic Systems

William B. Rouse

January 1981 **ACM C mputing Surveys (CSUR)**, Volume 13 Issue 1

Full text available: pdf(2.77 MB) Additional Information: full citation, abstract, references, citings, index terms

Modes of human-computer interaction in the control of dynamic systems are discussed, and the problem of allocating tasks between human and computer considered. Models of human performance in a variety of tasks associated with the control of dynamic systems are reviewed. These models are evaluated in the context of a design example involving human-computer interaction in aircraft operations. Other examples include power plants, chemical plants, and ships.

Keywords: aircraft, control, dynamic systems, human-computer interaction, mathematical models, system design, task analysis

13 A FPGA-based implementation of a fault-tolerant neural architecture for photon identification

M. Alderighi, E. L. Gummati, V. Piuri, G. R. Sechi

February 1997 **Proceedings of the 1997 ACM fifth international symposium on Field-programmable gate arrays**

Full text available: pdf(965.46 KB) Additional Information: full citation, references, citings, index terms

14 A knowledge-based approach for power system dynamic security assessment

B. Jeyasurya, S. S. Venkata

June 1990 **Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2**

Full text available: pdf(623.30 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a knowledge-based method for predicting the robustness of a power system to severe disturbances. The method builds decision trees using the attributes which are closely related to the stability of the power system. A simple power system is used to illustrate the important features of the proposed method.

15 Real-time disturbance control

B. Chandrasekaran, R. Bhatnager, D. D. Sharma

August 1991 **Communications of the ACM**, Volume 34 Issue 8

Full text available: pdf(3.75 MB) Additional Information: full citation, references, citings, index terms, review

16 Deep Sub-Micron IDDQ Testing: Issues and Solutions

M. Sachdev

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, citings

Publisher Site

The effectiveness of I/sub DDQ/ testing in deep sub-micron is threatened by the increased transistor sub-threshold leakage current. In this article, we survey possible solutions and propose a deep sub-micron I/sub DDQ/ test mode. The methodology provides means for unambiguous measurements of I/sub DDQ/ components and defect diagnosis. The effectiveness of the test mode is demonstrated with a real life example.

Keyw rds: CMOS integrated circuits, deep submicron IDDQ testing, transistor sub-threshold leakage current, defect diagnosis, CMOS IC

17 Knowledge based system to diagnose faults in discrete event systems
Muralidhar Sitaram, George Ernst, John Marcuse
June 1989 **Pr ceedings f the sec nd internati nal c nference n Industrial and engineering applicati ns f artificial intelligence and expert systems - Volume 1**
Full text available: pdf(405.96 KB) Additional Information: full citation, abstract, references, index terms

This paper describes a Fault Explanation System (FES) that aids in the diagnosis of failures in discrete event systems such as certain manufacturing processes. These systems are characterized by the use of programmable logic controllers (PLC) to control the systems. In addition PLC's also perform event logging. The event log (fault log) records exceptions which may be alarms, warnings or status reports. A major difficulty is that most of the alarms do not indicate real faults in the system; ...

18 Poster session: Application-dependent testing of FPGAs for bridging faults
Mehdi Baradaran Tahoori
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**
Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A new technique is presented for testing for bridging faults in the interconnects of an arbitrary design implemented in an FPGA. The configuration of the routing resources used in the original design remains unchanged in the test configurations. Only the logic blocks used in the design are reprogrammed in order to implement single-term functions, logic functions with only one minterm or one maxterm. As shown by formal proofs, all activated faults are detected when single-term functions and appro ...

19 On the experience of using cause-effect graphs for software specification and test generation
Amit Paradkar
October 1994 **Proceedings of the 1994 conference of the Centre for Advanced Studies on Collaborative research**
Full text available: pdf(51.57 KB) Additional Information: full citation, abstract, references, citings, index terms

The notion of cause-effect graphs (CEGs) has existed for more than two decades, but its use is not yet popular. In this paper, we describe several empirical studies of using cause-effect graphs for the specification and testing of real software, including a boiler control and monitor system, a set of N-version programs for navigation tracking, and a database monitoring system. We present the problems encountered in these empirical studies, the solutions developed to solve them, the evaluation of ...

20 Hierarchical representation and machine learning from faulty jet engine behavioral examples to detect real time abnormal conditions
U. K. Gupta, M. Ali
June 1988 **Proceedings of the first international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 2**
Full text available: pdf(991.31 KB) Additional Information: full citation, references, citings, index terms

Terms used **pump** and **artificial neural** and **fault** and **detect** and **power**

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21 System safety through automatic high-level code transformations: an experimental evaluation

P. Cheynet, B. Nicolescu, R. Velazco, M. Rebaudengo, M. Sonza Reorda, M. Violante

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(62.61 KB) Additional Information: full citation, references, index terms

22 Computing curricula 2001

September 2001 **Journal on Educational Resources in Computing (JERIC)**

Full text available: pdf(613.63 KB) html(2.78 KB) Additional Information: full citation, references, citings, index terms

23 Process control supervision using qualitative models

R. K. Stobart, N. R. Shadbolt

June 1990 **Proceedings of the third international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**

Full text available: pdf(752.28 KB) Additional Information: full citation, abstract, references, index terms

In modern process and power plant the cost of installation demands operation at peak efficiency for prolonged periods. This places significant demands on the control and monitoring systems to keep efficiency high while giving significant warning of a drop in efficiency or a component failure. We present an approach to process monitoring based on Qualitative Models which are used as a framework in which a range of monitoring techniques are located. The methods are described in the context of ...

24 Poster session: Wireless sensor networks: a power-scalable motion estimation IP for hybrid video coding

Federico Quaglio, Maurzio Martina, Fabrizio Vacca, Guido Masera, Andrea Molino, Gianluca Piccinini, Maurizio Zamboni

February 2003 **Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Wireless Sensor Networks are an emerging phenomenon in the research community. The design and development of network architectures and nodes implementation are fostering many research activities. Due to their wide application fields and pervasive employment possibilities, the investigation of novel classes of wireless sensor nodes is of great concern. In this paper we presented a novel Power-Scalable Motion Estimation IP suitable for video-surveillance over Wireless Sensor Networks. The proposed ...

25 Poster session: An automated and power-aware framework for utilization of IP cores in hardware generated from C descriptions targeting FPGAs

Alex Jones, Prith Banerjee

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Use of hand optimized Intellectual Property (IP) logic cores is prolific in hardware design. While IP cores remain a standard way to utilize the improvement in FPGA technology and contend with time to market pressure through reuse, popularity of tools generating hardware descriptions from high-level languages is also increasing in popularity. PACT HDL combines these two methods within a power-aware framework. The PACT HDL compiler generates power optimized VHDL/Verilog from a C language descript ...

26 Poster session: Power-aware architectures and circuits for FPGA-based signal processing

Frank Honoré, Ben Calhoun, Anantha Chandrakasan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This work showcases a power-aware system design methodology for DSP applications on reconfigurable hardware platforms. In particular, an enhanced FPGA architecture is proposed and analyzed for a deep submicron process technology. These enhancements reduce Configurable Logic Block (CLB) usage for distributed arithmetic implementations of signal processing applications by 50% or more thereby reducing the load on interconnect resources. Multi-Threshold CMOS (MTCMOS) circuit design techniques are ag ...

27 Oracles for checking temporal properties of concurrent systems

Laura K. Dillon, Qing Yu

December 1994 **ACM SIGSOFT Software Engineering Notes , Proceedings of the 2nd ACM SIGSOFT symposium on Foundations of software engineering,** Volume 19 Issue 5

Full text available: pdf(1.30 MB) Additional Information: full citation, abstract, references, citings, index terms

Verifying that test executions are correct is a crucial step in the testing process. Unfortunately, it can be a very arduous and error-prone step, especially when testing a concurrent system. System developers can therefore benefit from oracles automating the verification of test executions.This paper examines the use of Graphical Interval Logic (GIL) for specifying temporal properties of concurrent systems and describes a method for constructing oracles from GIL specifications. The visually int ...

28 Poster session: A four-bit full adder implemented on fast SiGe FPGAs with novel power control scheme

K. Zhou, M. Chu, C. You, J.-R. Guo, Channakeshav, J. Mayega, B. S. Goda, R. P. Kraft, J. F. McDonald

February 2003 **Pr ceedings f the 2003 ACM/SIGDA eleventh international symposium n Field pr grammable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The low operating speed of current CMOS Field Programmable Gate Arrays (FPGAs), i.e., 10-220 MHz, has prevented their use in high-speed digital applications. With the advent of IBM Silicon Germanium (SiGe) 7HP technology, designers have been able to design FPGAs operating in the gigahertz range. This paper is going to elaborate on the implementation of a 4-bit ripple-carry full adder (FA) on the new SiGe FPGA with new architectures and a novel power management strategy. The 1-bit FA can be reali ...

29 Computer system reliability and nuclear war

Alan Borning

February 1987 **Communications of the ACM**, Volume 30 Issue 2

Full text available: pdf(2.50 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Given the devastating consequences of nuclear war, it is appropriate to look at current and planned uses of computers in nuclear weapons command and control systems, and to examine whether these systems can fulfill their intended roles.

30 Applications of machine learning and rule induction

Pat Langley, Herbert A. Simon

November 1995 **Communications of the ACM**, Volume 38 Issue 11

Full text available: pdf(554.28 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Machine learning is the study of computational methods for improving performance by mechanizing the acquisition of knowledge from experience. Expert performance requires much domain-specific knowledge, and knowledge engineering has produced hundreds of AI expert systems that are now used regularly in industry. Machine learning aims to provide increasing levels of automation in the knowledge engineering process, replacing much time-consuming human activity with automatic tec ...

31 Computer simulation and applications: Signal processing technique utilising fourier transform methods and Artificial Neural Network pattern recognition for interpreting complex data from a multipoint optical fibre sensor system

D. King, W. B. Lyons, C. Flanagan, E. Lewis

January 2004 **Proceedings of the winter international synposium on Information and communication technologies**

Full text available: pdf(148.20 KB) Additional Information: full citation, abstract, references

A multipoint (2 sensing elements) optical fibre based sensor system capable of detecting ethanol in water supplies is presented. The active sensing elements consist of an exposed core U-bend configuration in order to maximise sensitivity and the sensing system is interrogated using Optical Time Domain Reflectometry (OTDR). Artificial Neural Network (ANN) Pattern Recognition techniques have been applied to the optical fibre sensor system data in order to accurately classify each sensor element te ...

32 Temperature and power aware architectures: Routine based OS-aware microprocessor resource adaptation for run-time operating system power saving

Tao Li, Lizy Kurian John

August 2003 **Proceedings f the 2003 international symposium n L w p wer electr nics and design**

Full text available: pdf(385.70 KB) Additional Information: full citation, abstract, references, index terms

The increasingly constrained power budget of today's microprocessor has resulted in a situation where power savings of all components in a system have to be taken into consideration. Operating System (OS) is a major power consumer in many modern

applications execution. This paper advocates a routine based OS-aware microprocessor resource adaptation mechanism targeting run-time OS power savings. Simulation results show that compared with the existing sampling-based adaptation schemes, this novel ...

Keyw rds: adaptive processor, low power, operating system

33 Fault detection and input stimulus determination for the testing of analog integrated circuits based on power-supply current monitoring

Georges Gielen, Zhihua Wang, Willy Sansen

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(451.00 KB) Additional Information: full citation, abstract, references, citings, index terms

A new method for the testing and fault detection of analog integrated circuits is presented. Time-domain testing followed by spectral analysis of the power-supply current is used to detect both DC and AC faults. Spectral analysis is applied since the tolerances on the circuit parameters make a direct comparison of waveforms impossible. For the fault detection a probabilistic decision rule is proposed based on a multivariate statistical analysis. Since no extra testing pin is needed and the ...

34 Detecting undetectable controller faults using power analysis

J. Carletta, C. A. Papachristou, M. Nourani

January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(120.16 KB) Publisher Site Additional Information: full citation, references, index terms

35 New test methods targeting non-classical faults: Embedded software-based self-testing for SoC design

A. Krstic, W. C. Lai, K. T. Cheng, L. Chen, S. Dey

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(324.94 KB) Additional Information: full citation, abstract, references, index terms

At-speed testing of high-speed circuits is becoming increasingly difficult with external testers due to the growing gap between design and tester performance, growing cost of high-performance testers and increasing yield loss caused by inherent tester inaccuracy. Therefore, empowering the chip to test itself seems like a natural solution. Hardware-based self-testing techniques have limitations due to performance and area overhead and problems caused by the application of non-functional patterns. ...

Keywords: SoC test, VLSI test, functional test, microprocessor test

36 The role of artificial intelligence in fault-tolerant process-control systems

F. B. Bastani, I.-R. Chen

June 1988 **Proceedings of the first international conference on Industrial and engineering applicati ns f artificial intelligence and expert systems - V lume 2**

Full text available: pdf(854.81 KB) Additional Information: full citation, references, citings, index terms

37 Optimizing amplifier placements in a multiwavelength optical LAN/MAN: the unequally

powered wavelengths case
Byrav Ramamurthy, Jason Iness, Biswanath Mukherjee
December 1998 **IEEE/ACM Transacti ns n Netw rking (TON)**, Volume 6 Issue 6
Full text available: pdf(413.51 KB) Additional Information: full citation, references, index terms

Keywords: WDM, amplifier placement, linear-nonlinear programming, local area network/metropolitan area network, optical network, optimization, passive star

38 Hazard identification in programmable system: a methodology and case study
E. J. Broomfield, P. W. H. Chung
March 1994 **ACM SIGAPP Applied Computing Review**, Volume 2 Issue 1
Full text available: pdf(621.30 KB) Additional Information: full citation, abstract, index terms

This paper describes the application of a methodology developed to meet the need for hazard identification in programmable systems. The methodology was derived using real incident data and assesses the safety of a system by decomposing high level requirements into *tasks*. The tasks are analysed using a new graphical technique and the safety of tasks is assessed by using *attributes/guide-words* and associated *questions*. A case study is used to examine the effectiveness and feas ...

Keywords: HAZOP, hazard identification, incidents, safety

39 Utilizing multilevel models and reasoning for diagnosis of a complex electro-mechanical system
John A. Smith, Gautam Biswas
June 1989 **Proceedings of the second international conference on Industrial and engineering applications of artificial intelligence and expert systems - Volume 1**
Full text available: pdf(919.69 KB) Additional Information: full citation, abstract, references, citings, index terms

A multi-level system which utilizes both an evidential and a qualitative model for diagnosing fault symptoms in complex electro-mechanical systems is presented. The operation of both models, enhancement by a historical database, and the global control strategy are all discussed. In addition, the constraining of qualitative reasoning with information from the evidential session and the enhancement of the evidential model with information from the qualitative model is demonstrated

40 The use of the electrical simulator SPICE for behavioral simulation of artificial neural networks
Vincenzo Piuri
April 1991 **Proceedings of the 24th annual symposium on Simulation**
Full text available: pdf(1.27 MB) Additional Information: full citation, references, index terms

Terms used **pump** and **artificial neural** and **fault** and **detect** and **power**

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41 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

42 Fast timing simulation of transient faults in digital circuits

A. Dharchoudhury, S. M. Kang, H. Cha, J. H. Patel

November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(362.04 KB) Additional Information: full citation, abstract, references, index terms

Transient fault simulation is an important verification activity for circuits used in critical applications since such faults account for over 80% of all system failures. This paper presents a timing level transient fault simulator that bridges the gap between electrical and gate-level transient fault simulators. A generic MOS circuit primitive and analytical solutions of node differential equations are used to perform transistor level simulation with accurate MOS-FET models. The transient ...

43 Energy-aware system design: A survey of techniques for energy efficient on-chip communication

Vijay Raghunathan, Mani B. Srivastava, Rajesh K. Gupta
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(94.50 KB) Additional Information: full citation, abstract, references, citings, index terms

Interconnects have been shown to be a dominant source of energy consumption in modern day System-on-Chip (SoC) designs. With a large (and growing) number of electronic systems being designed with battery considerations in mind, minimizing the energy consumed in on-chip interconnects becomes crucial. Further, the use of nanometer technologies is making it increasingly important to consider reliability issues during the design of SoC communication architectures. Continued supply voltage scaling ha ...

Keywords: communication architectures, energy efficient design, low power design, power management, system-on-chip design

44 Poster session: A high resolution diagnosis technique for open and short defects in FPGA interconnects

Mehdi Baradaran Tahoori
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

A two-step diagnosis flow, coarse-grain and fine-grain, is presented in order to identify a faulty element in the FPGA interconnects. The fault models used for interconnect are open, resistive-open, and bridging fault. The coarse-grain phase identifies the faulty net, the routing between two consecutive sequential elements in the FPGA. This phase is performed by just post-processing tester results for the test configurations used for interconnect testing. During the fine-grain step, the faulty n ...

45 Poster session: Design of a fingerprint system using a hardware/software environment

Lee Vanderlei Bonato, Rolf Fredi Molz, João Carlos Furtado, Marcos Flores Ferrão, Fernando G. Moraes
February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Processing system of fingerprint are CPU time intensive, being normally implemented in software. This paper present a new algorithm for fingerprint features localization, that can be easily implemented in hardware (system-on-a-chip, FPGA). This algorithm is composed by 3 stages, first stage read a fingerprint image (255x255pixels, ash tones) and apply a Gaussian Filter, after this, apply a absolute difference mask (ADM) for detector the edges in the image filtered and the last stage look for fin ...

46 Technique for automatically correcting words in text

Karen Kukich
December 1992 **ACM Computing Surveys (CSUR)**, Volume 24 Issue 4

Full text available: pdf(6.23 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Research aimed at correcting words in text has focused on three progressively more difficult problems:(1) nonword error detection; (2) isolated-word error correction; and (3) context-dependent work correction. In response to the first problem, efficient pattern-matching and n-gram analysis techniques have been developed for detecting strings that do not appear in a given word list. In response to the second problem, a variety of general and application-specific spelling cor ...

Keywords: n-gram analysis, Optical Character Recognition (OCR), context-dependent spelling correction, grammar checking, natural-language-processing models, neural net classifiers, spell checking, spelling error detection, spelling error patterns, statistical-language models, word recognition and correction

47 Poster session: FPGA-based design of an evolutionary controller for collision-free robot navigation

M. A. H. B. Azhar, K. R. Dimond

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The employment of field programmable gate arrays (FPGAs) to a robot controller is very attractive, since it allows for fast IC prototyping and low cost modifications. The speedup is achieved because of pipelining and dedicated functions in hardware that are customized to the problem. The self learning ability and the adaptive nature of an Artificial Neural Network (ANN) makes it a good candidate for the control structure of a robot's navigation. An evolutionary approach in designing robots can e ...

48 The Datacycle architecture

T. F. Bowen, G. Gopal, G. Herman, T. Hickey, K. C. Lee, W. H. Mansfield, J. Raitz, A. Weinrib

December 1992 **Communications of the ACM**, Volume 35 Issue 12

Full text available: pdf(3.91 MB) Additional Information: full citation, references, citings, index terms, review

Keywords: VLSI filtering, concurrency control, data filtering, database architectures, database machines, fuzzy queries, high performance, transaction processing

49 High-pressure steam engines and computer software

Nancy G. Leveson

June 1992 **Proceedings of the 14th international conference on Software engineering**

Full text available: pdf(1.40 MB) Additional Information: full citation, references, citings, index terms

50 Poster session: On computation and resource management in an FPGA-based computation environment

Soheil Ghiasi, Karlene Nguyen, Elaheh Bozorgzadeh, Majid Sarrafzadeh

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract, citings

The idea of managing the comprising computations of an application executed in an FPGA-based system is presented. An efficient algorithm for exploiting the timing slack of building blocks of the application is proposed. The slack of these blocks can be utilized by replacing them with slower but "cheaper" modules and by assigning the computations to the proper resources. Thus, our approach manages the comprising computations and system resources at the same time. This is performed without comprom ...

51 Poster session: A physical retiming algorithm for field programmable gate arrays

Peter Suaris, Dongsheng Wang, Pei-Ning Guo, Nan-Chi Chou

February 2003 **Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In this paper, we present a physical retiming algorithm for sequential circuits implemented in field programmable gate arrays (FPGAs). This algorithm can speed up the sequential circuits by reducing delay of all critical paths with negative slacks. By taking advantage of the physical information provided by placed circuits, this algorithm integrates two operations: retiming and register duplication. Retiming moves registers across combinational components. Register duplication moves registers ac ...

52 Poster session: Design strategies and modified descriptions to optimize cipher FPGA implementations: fast and compact results for DES and triple-DES

Gaël Rouvroy, Francois-Xavier Standaert, Jean-Jacques Quisquater, Jean-Didier Legat

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

We propose a new mathematical DES description that allows optimized implementations. It also provides the best DES and triple-DES FPGA implementations known in term of ratio throughput/area, where area means the number of FPGA slices used. First, we get a less resource consuming unrolled DES implementation that works at data rates of 21.3 Gbps (333 MHz), using VIRTEX II technology. In this design, the plaintext, the key and the mode (encryption/decrytion) can be changed on a cycle-by-cycle basis ...

53 Poster session: Lattice adaptive filter implementation for FPGA

Zdenek Pohl, Rudolf Matoušek, Jirí Kadlec, Milan Tichý, Miroslav Lícko

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Our poster introduces an innovative RLS Lattice filter implementation for FPGAs. The signal processing applications typically require wide numeric range, and that poses a problem when using an FPGA implementation. Our approach is based on arithmetic using logarithmic numeric representation (LNS). The test application - an adaptive noise canceller - has been optimized for the Xilinx Virtex devices. It consumes roughly 70% of all logic resources of the XCV800 device and all block memory cells. The ...

54 Poster session: An FPGA architecture with built-in error correction capability

P. K. Lala, B. Kiran Kumar

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The use of very deep submicron technology makes VLSI-based digital systems more susceptible to transient or soft errors, and thus compromises their reliability. This paper proposes an FPGA architecture inspired by the human immune system that allows tolerance of transient errors. The architecture is composed of a two-dimensional array of identical functional cells with different genetic codes. These codes are chosen based on the required functions to be performed by the functional cells. An erro ...

55 Poster session: Synthetic circuit generation using clustering and iteration

Paul D. Kundarewich, Jonathan Rose

February 2003 **Pr ceedings f the 2003 ACM/SIGDA eleventh internati nal symp sium n Field pr grammable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

The development of next-generation CAD tools and FPGA architectures requires benchmark circuits to experiment with new algorithms and architectures. There has always been a

shortage of good public benchmarks for these purposes, and even companies that have access to proprietary customer designs could benefit from designs that meet size and other particular specifications. In this paper, we present a new method of generating realistic synthetic benchmark circuits to help alleviate this shortage. ...

56 Poster session: Reconfigurable randomized K-way graph partitioning

Fatih Kocan

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

In this paper, a randomized k-way graph partitioning algorithm is mapped onto reconfigurable hardware. The randomized algorithm relies on repetitive running of the same algorithm with different random number sequences to achieve the (near-)optimal solution. The run-time and hardware requirements of this reconfigurable solution per a random number sequence are O(|V|-K) cycles and O(|V|log|V|+|E|) gates and flip-flops, respectively. Performance is improved further at the expense of more hardware b ...

57 Poster session: FPGAs in critical hardware/software systems

Adrian J. Hilton J. Adrian J. Hilton, Gemma Townson, Jon G. Hall

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

FPGAs are being used in increasingly complex roles in critical systems, interacting with conventional critical software. Established safety standards require rigorous justification of safety and correctness of the conventional software in such systems. Newer standards now make similar requirements for safety-related electronic hardware, such as FPGAs, in these systems. In this paper we examine the current state-of-the-art in programming FPGAs, and their use in conventional (low-criticality) hard ...

58 Poster session: A SC-based novel configurable analog cell

Binlin Guo, Jiarong Tong

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

This paper presents a high performance Configurable Analog Cell (CAC) which is made up of a Basic Configurable Analog Cell (BCAC) and a digital converter block. The CAC can be used either for Field Programmable Analog Array (FPAA) or for Field Programmable Digital-Analog Mixed Array (FPMA). The BCAC include three innovative Programmable Switch Blocks (PSBs), three Programmable Capacitor Arrays (PCAs), and an amplifier. PSB and PCA can be programmed to generate many equivalent components. In addi ...

59 Poster session: Testing for bit error rate in FPGA communication interfaces

Yongquan Fan, Zeljko Zilic

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

FPGAs have witnessed an increased use of dedicated communication interfaces. With their increased use, it is becoming critical to test and properly characterize all such interfaces. Bit error rate (BER) characteristic is one of the basic measures of the performance of any digital communication system. We propose a scheme for BER testing in FPGAs, which exhibits a few orders of magnitude speedup compared to traditional software simulation methods. In this scheme, we include a novel implementation ...

60 Poster session: On hiding latency in reconfigurable systems: the case of merge-sort for an FPGA-based system

Hossam ElGindy, George Ferizis

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(187.05 KB) Additional Information: full citation, abstract

Recursive solutions are effective software techniques that are difficult to map into hardware due to their dependency on input size and data values. As a result, most high-level design tools do not allow for recursive calls. In this paper we present a technique for mapping the merge-sort algorithm, as a case study, into a reconfigurable system. Our mapping employs an on-line prediction method to reconfigure the necessary hardware only when the need arises, and to hide the reconfiguration delay. ...

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